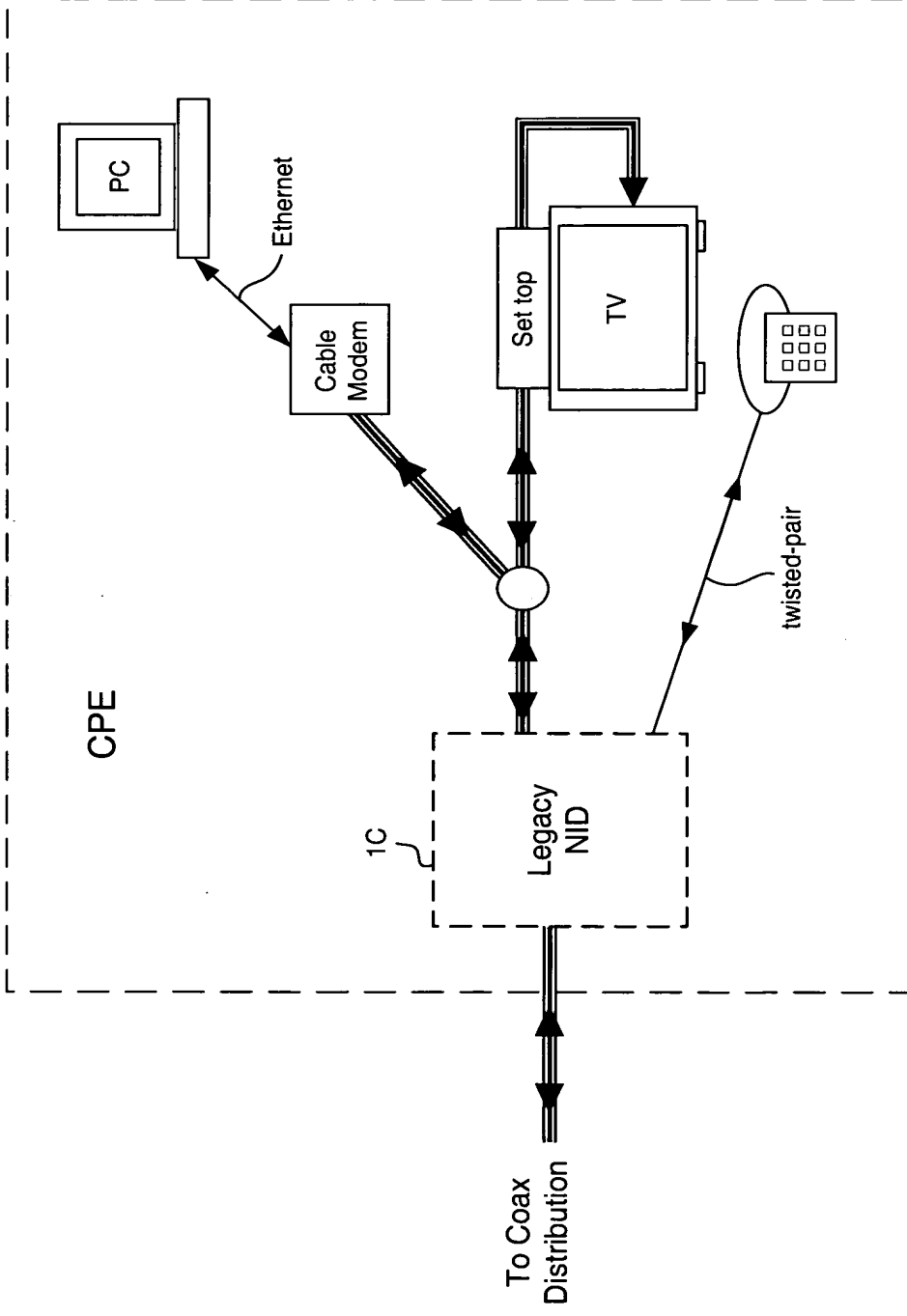
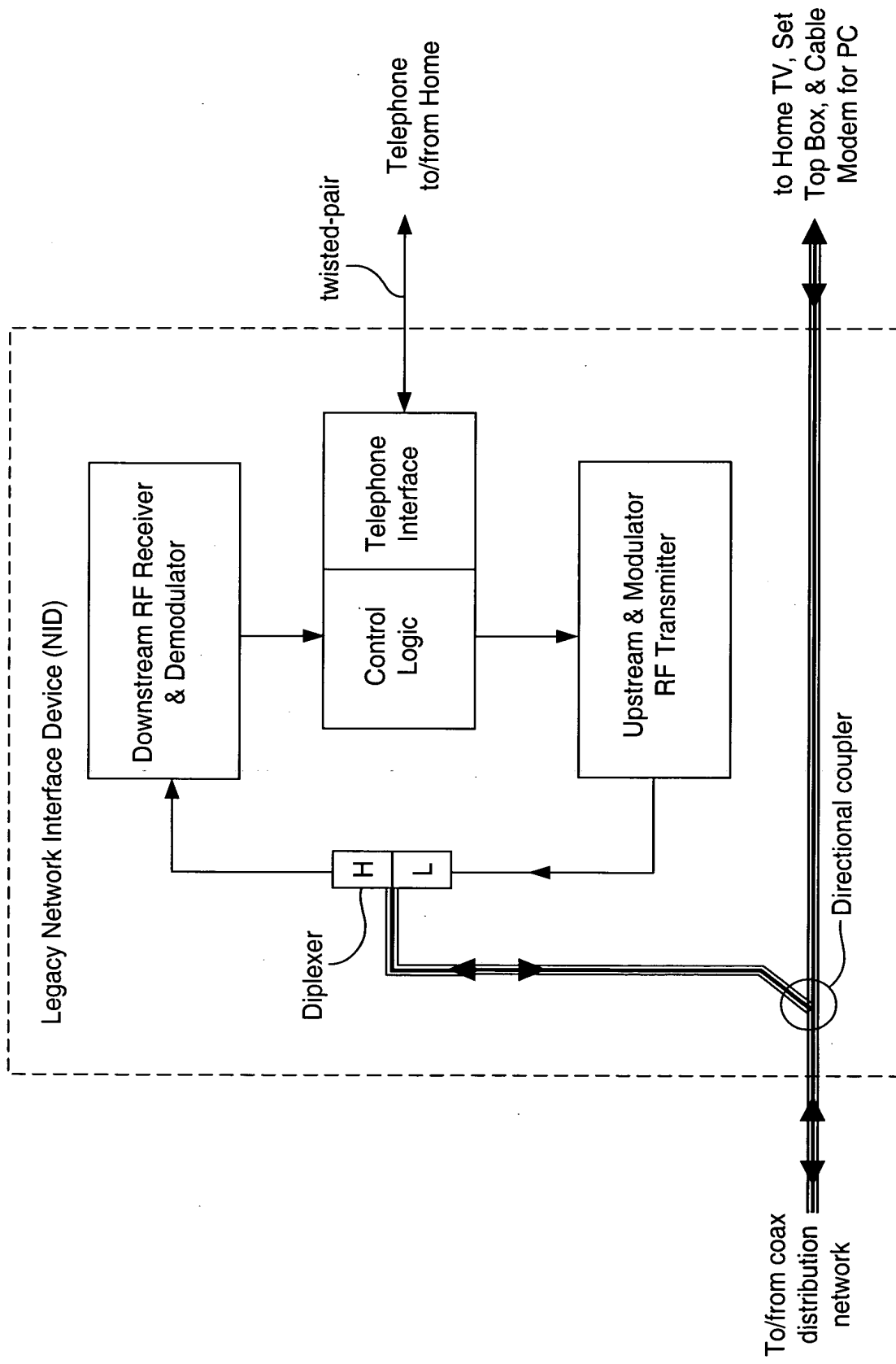


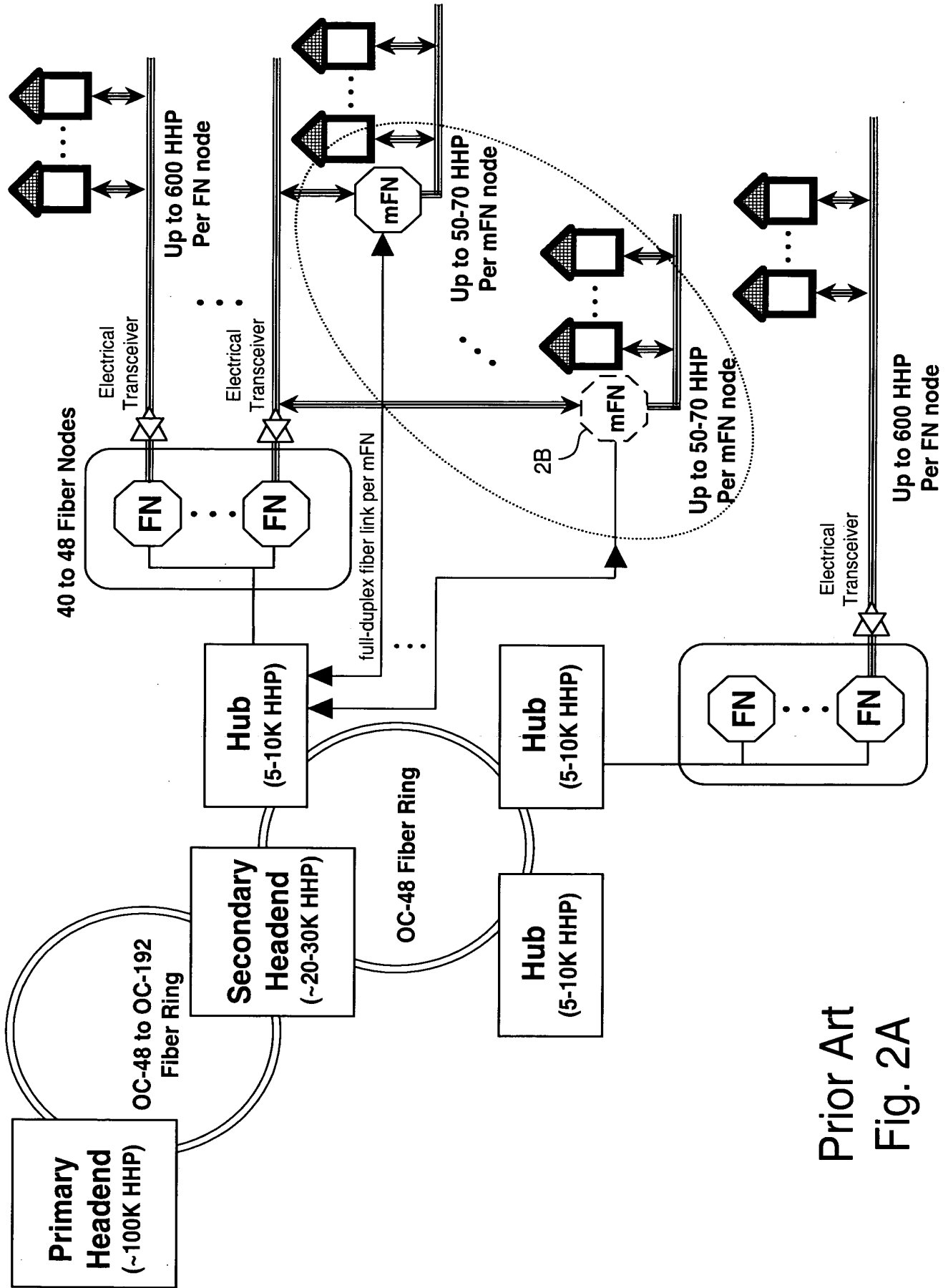
Prior Art
Fig. 1A



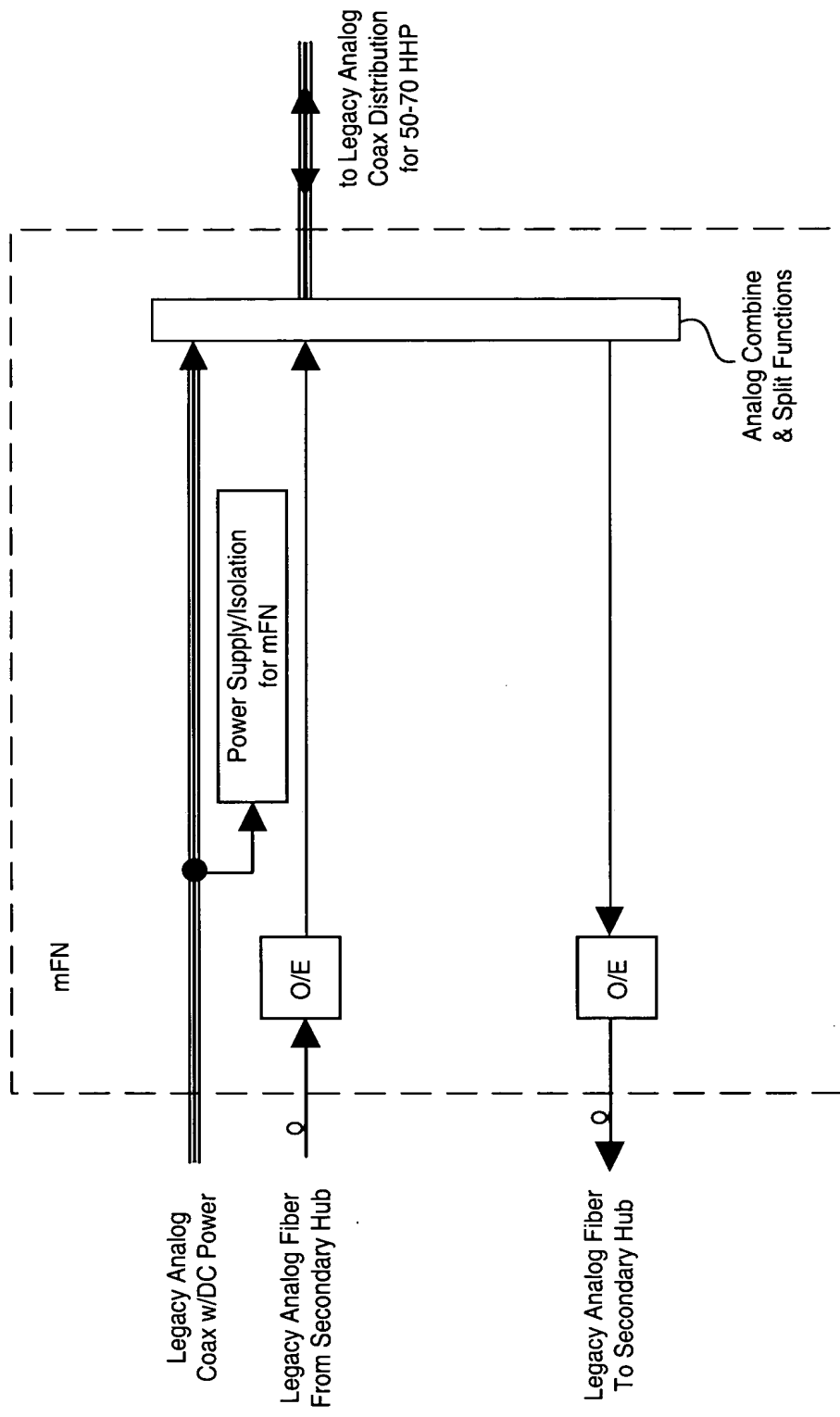
Prior Art
Fig. 1B



Prior Art
Fig. 1C



Prior Art
Fig. 2A



Prior Art
Fig. 2B

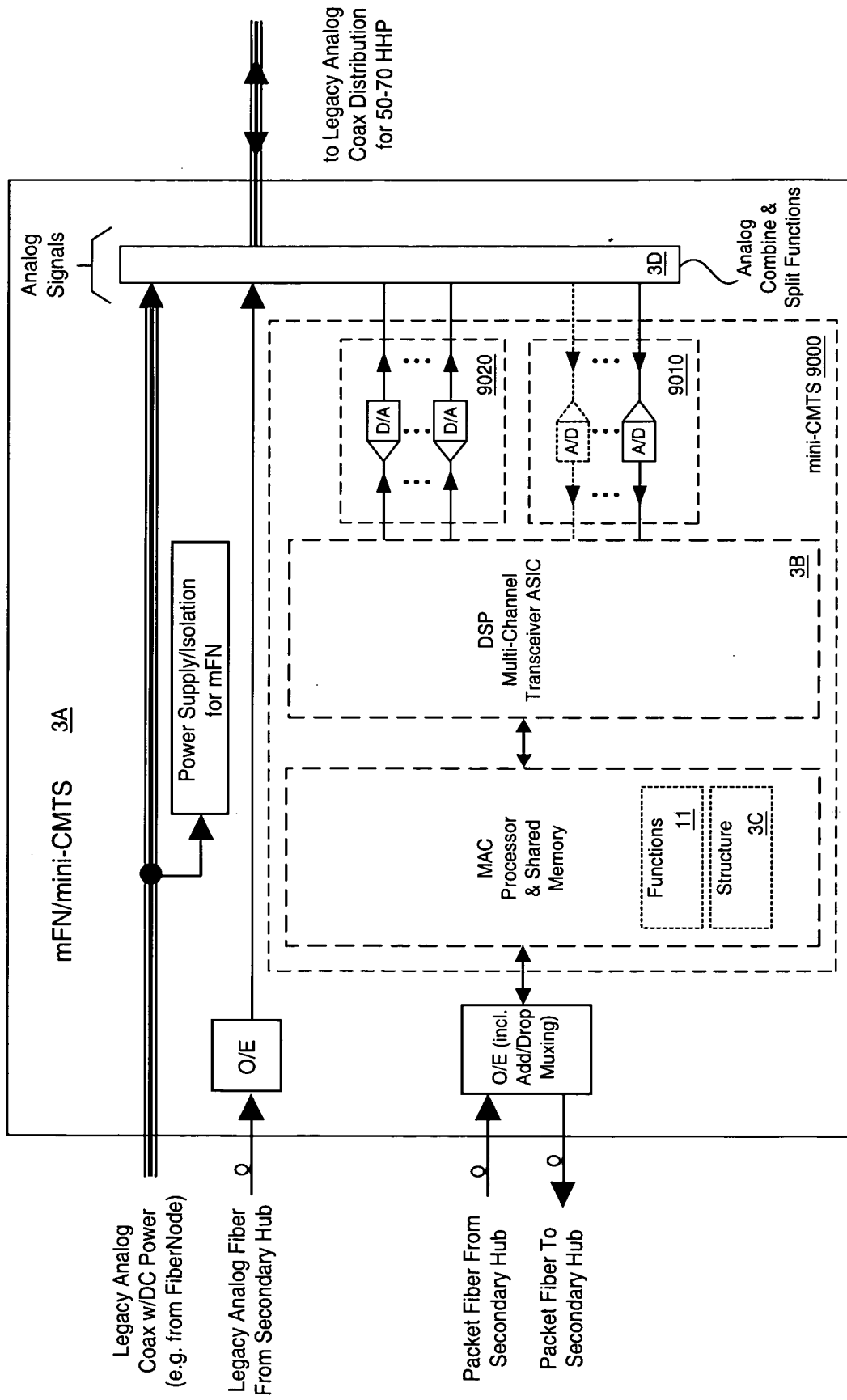


Fig. 3A

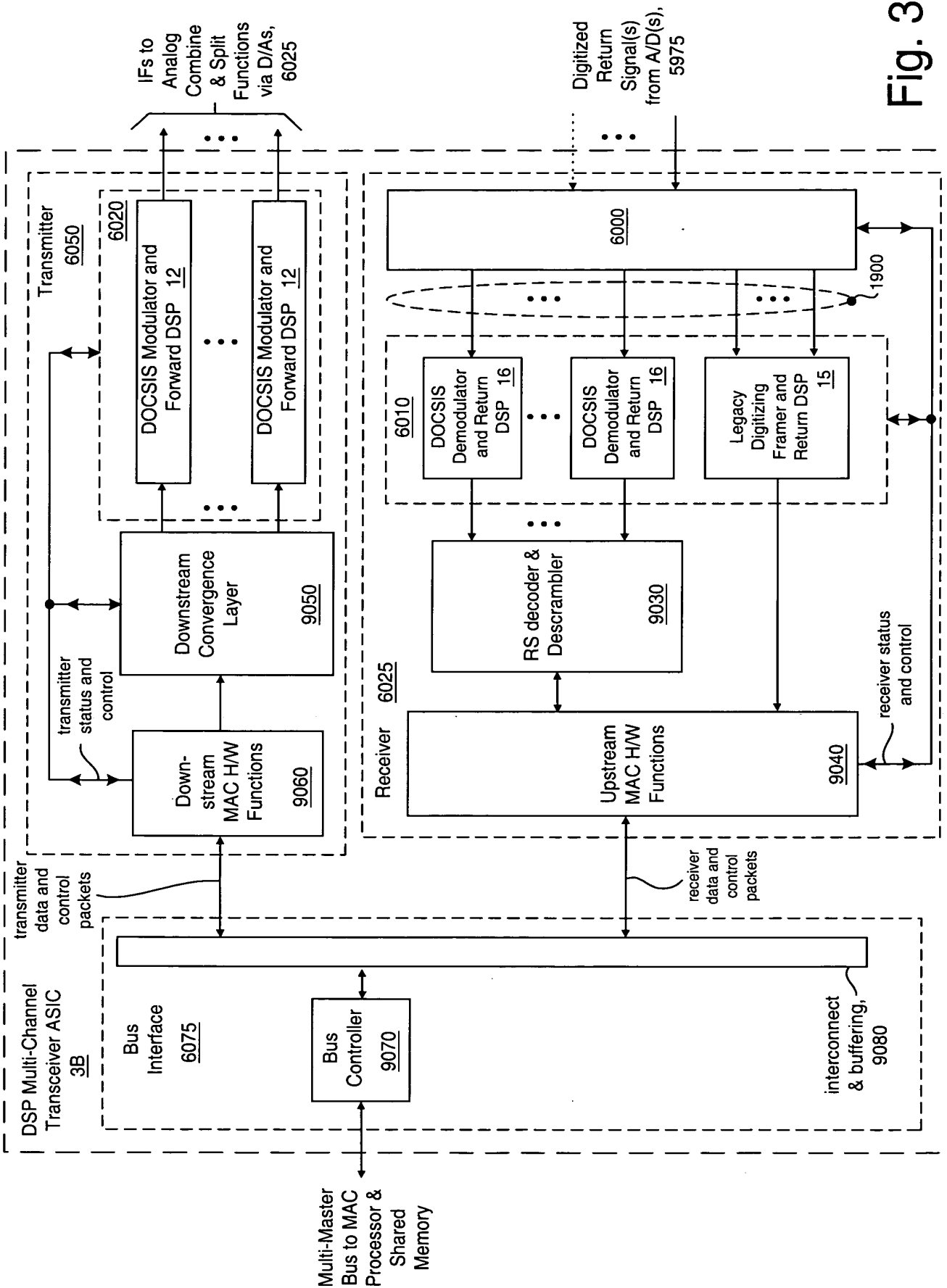


Fig. 3B

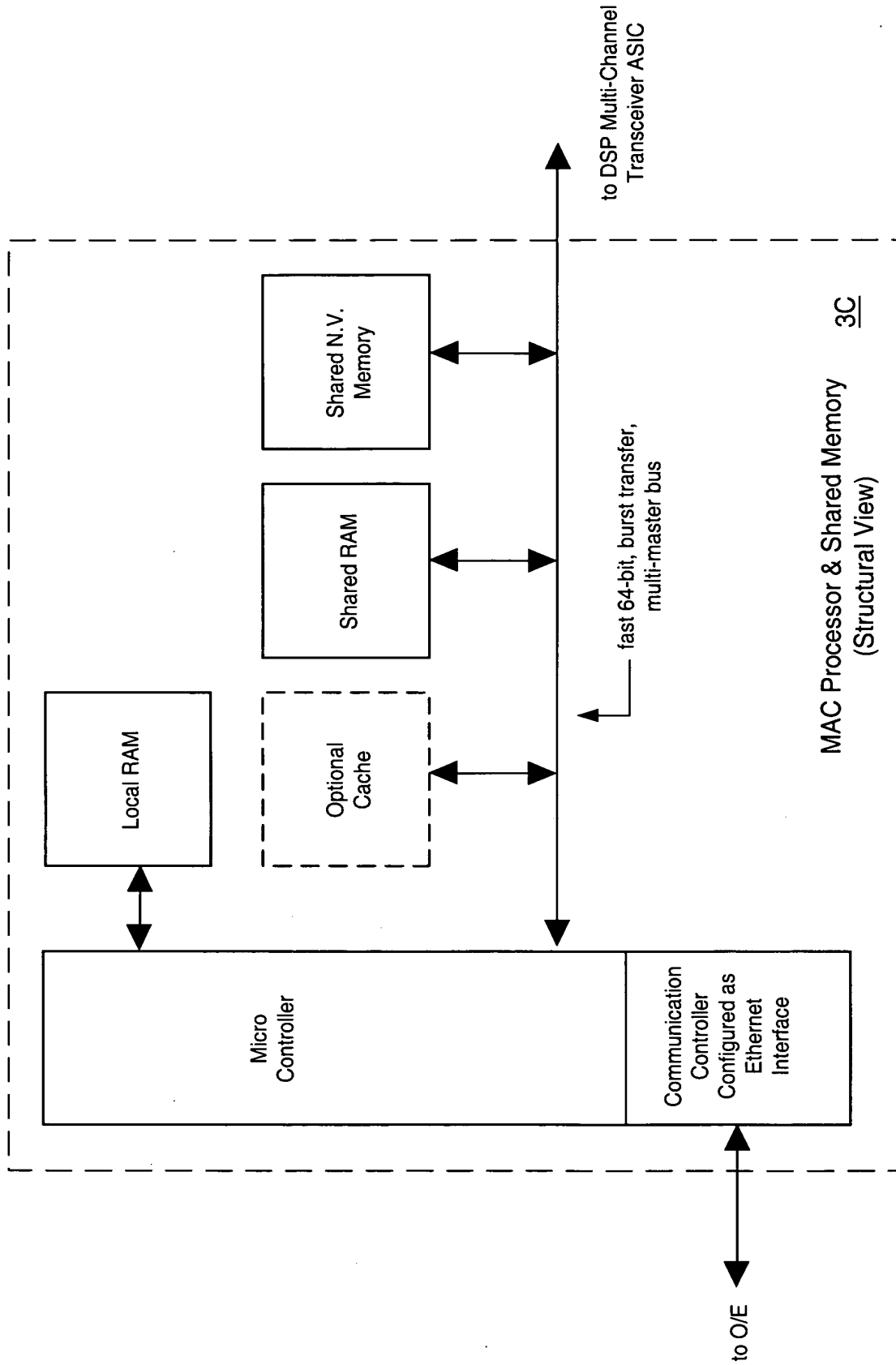


Fig. 3C

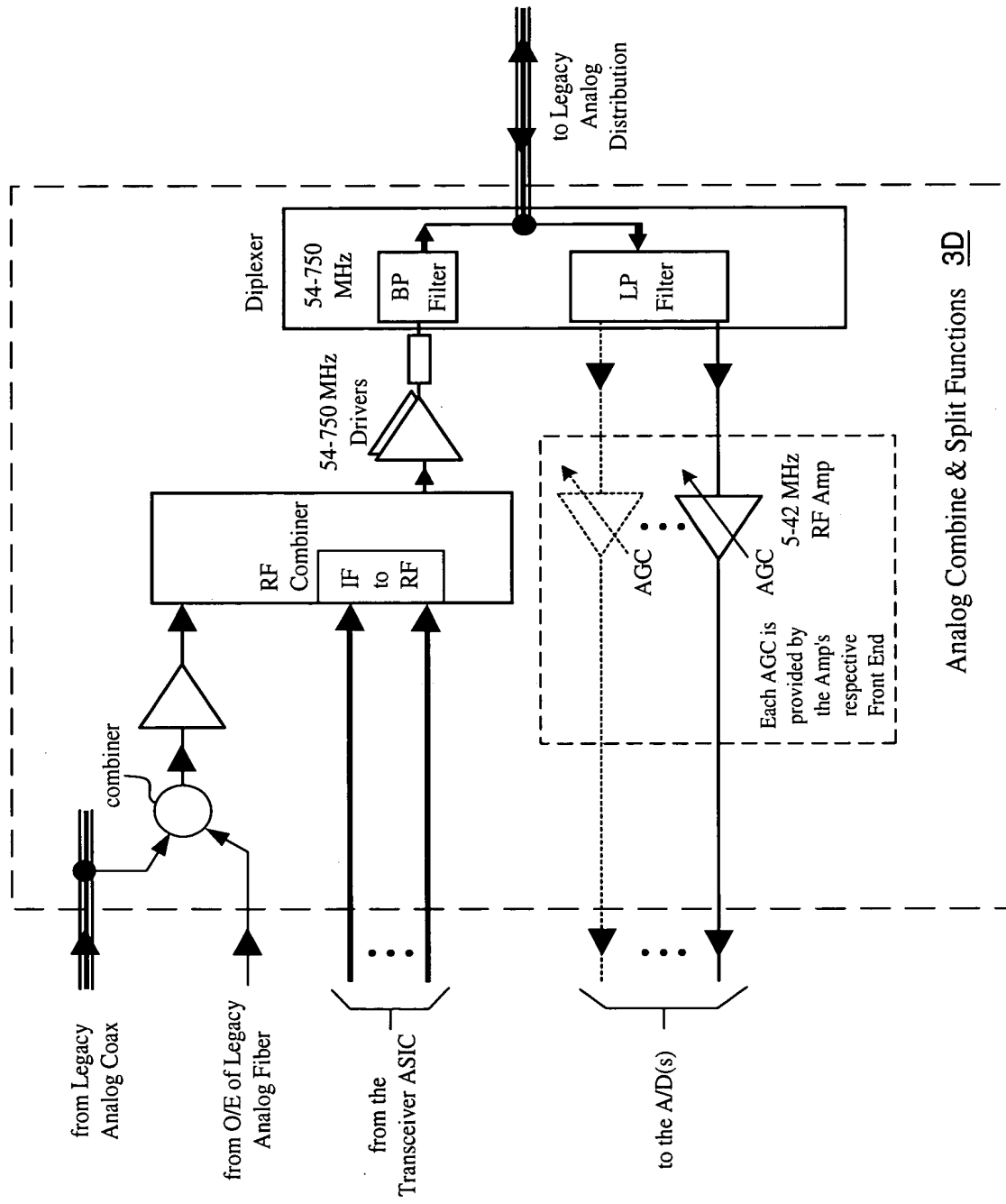


Fig. 3D

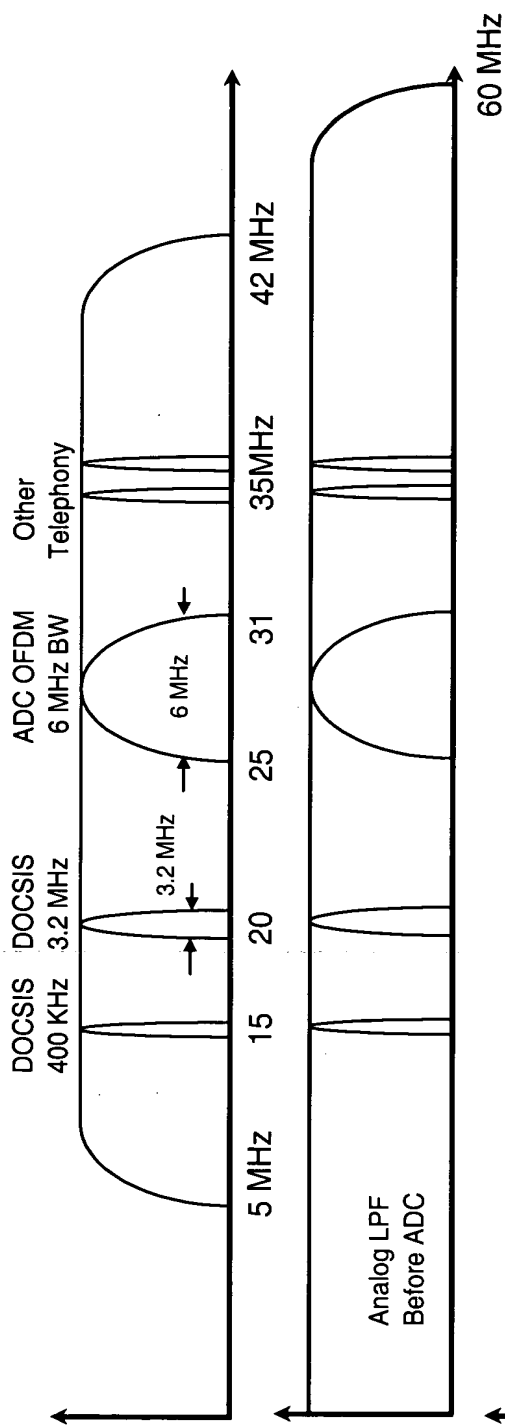


Fig. 4A

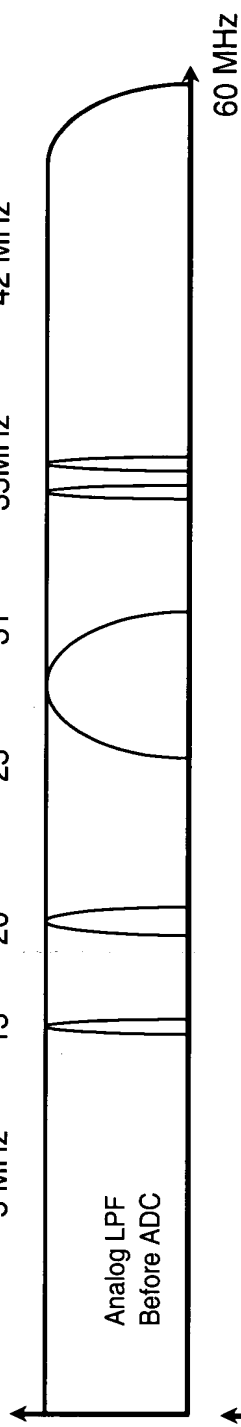


Fig. 4B

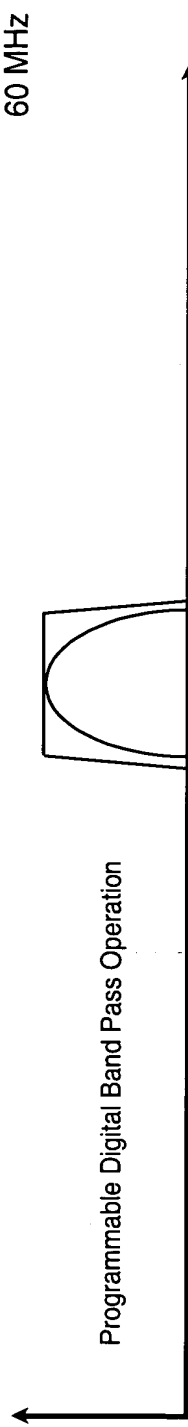


Fig. 4C

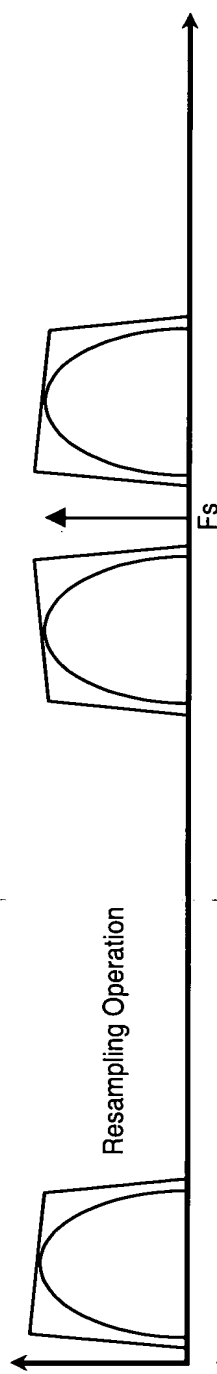


Fig. 4D

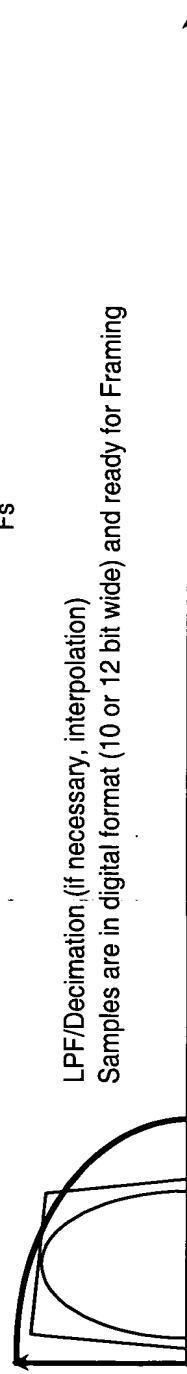


Fig. 4E

LPF/Decimation (if necessary, interpolation)
Samples are in digital format (10 or 12 bit wide) and ready for Framing

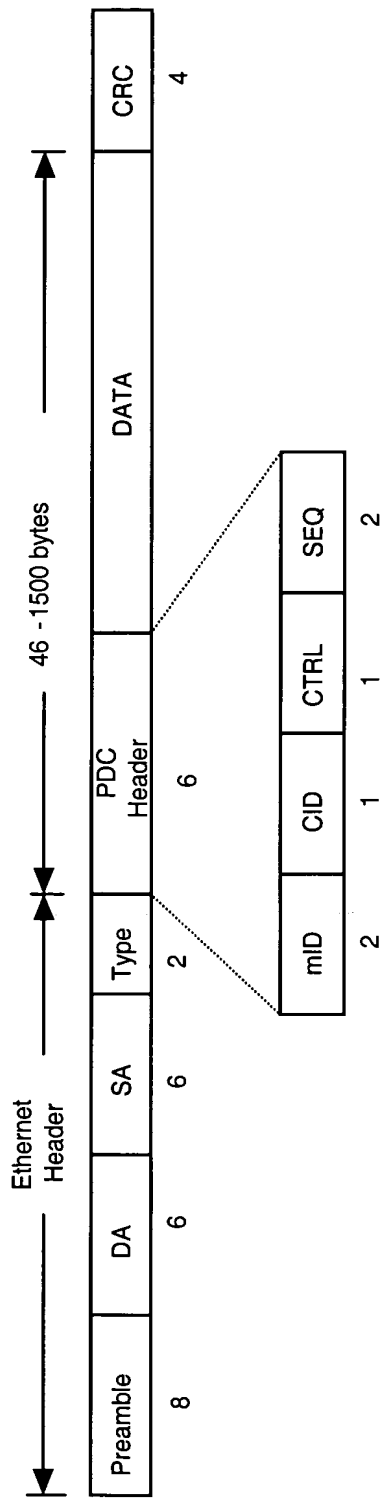


Fig. 5

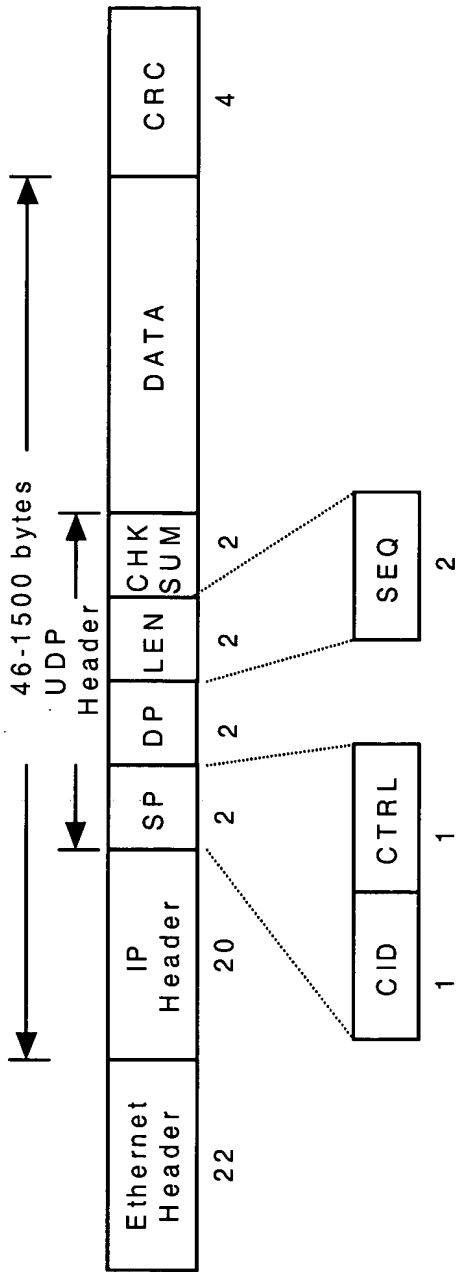


Fig. 6

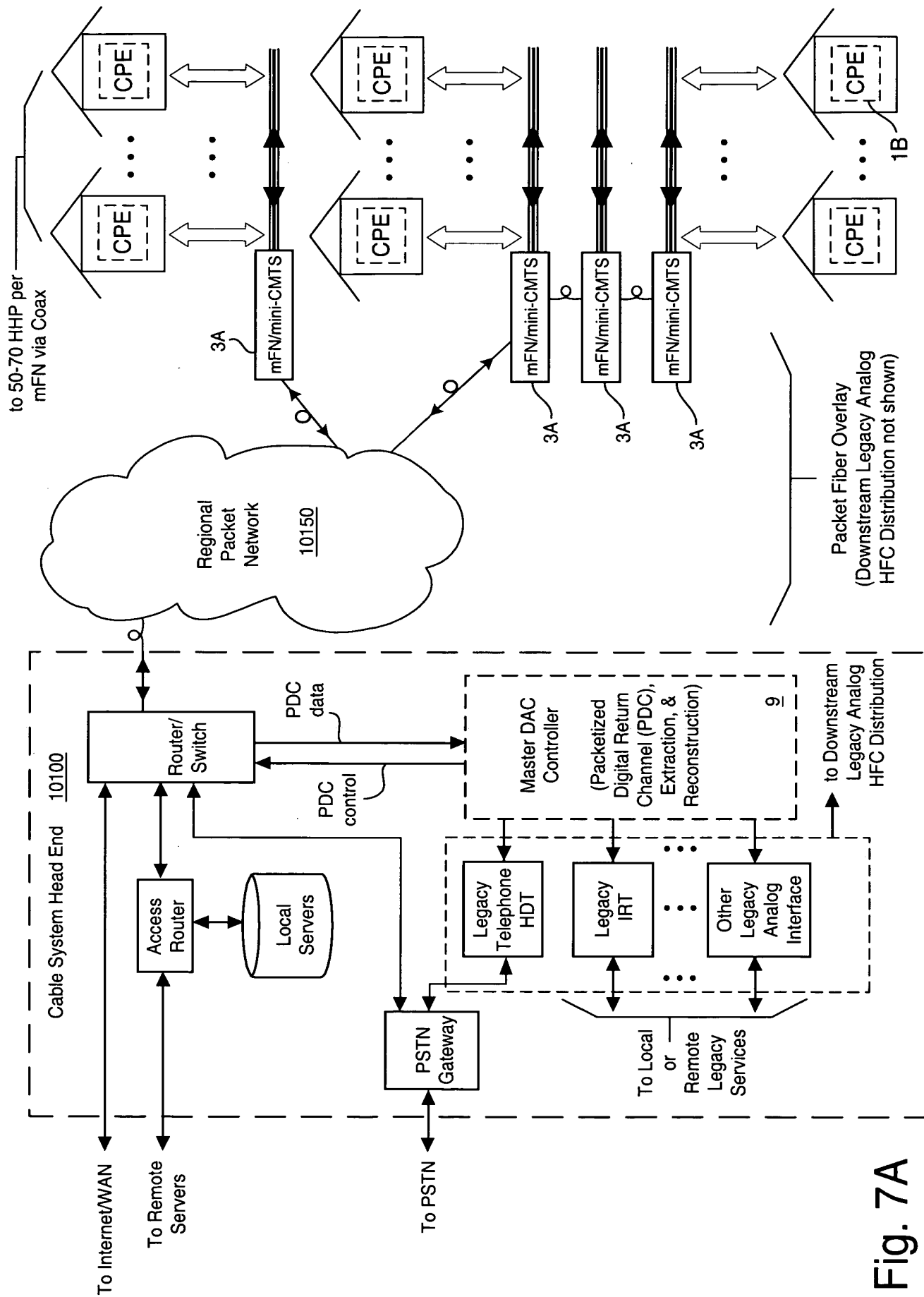


Fig. 7A

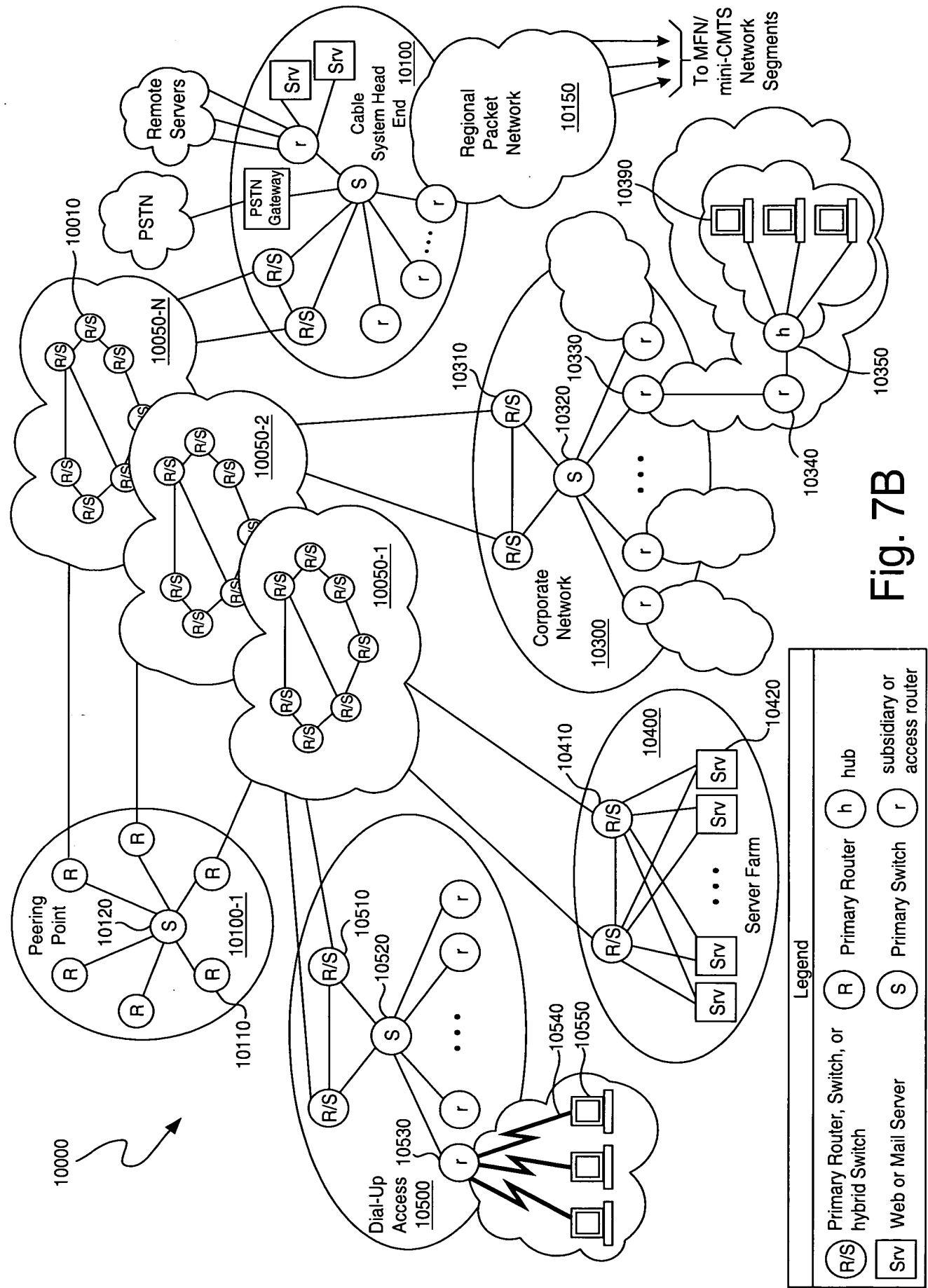


Fig. 7B

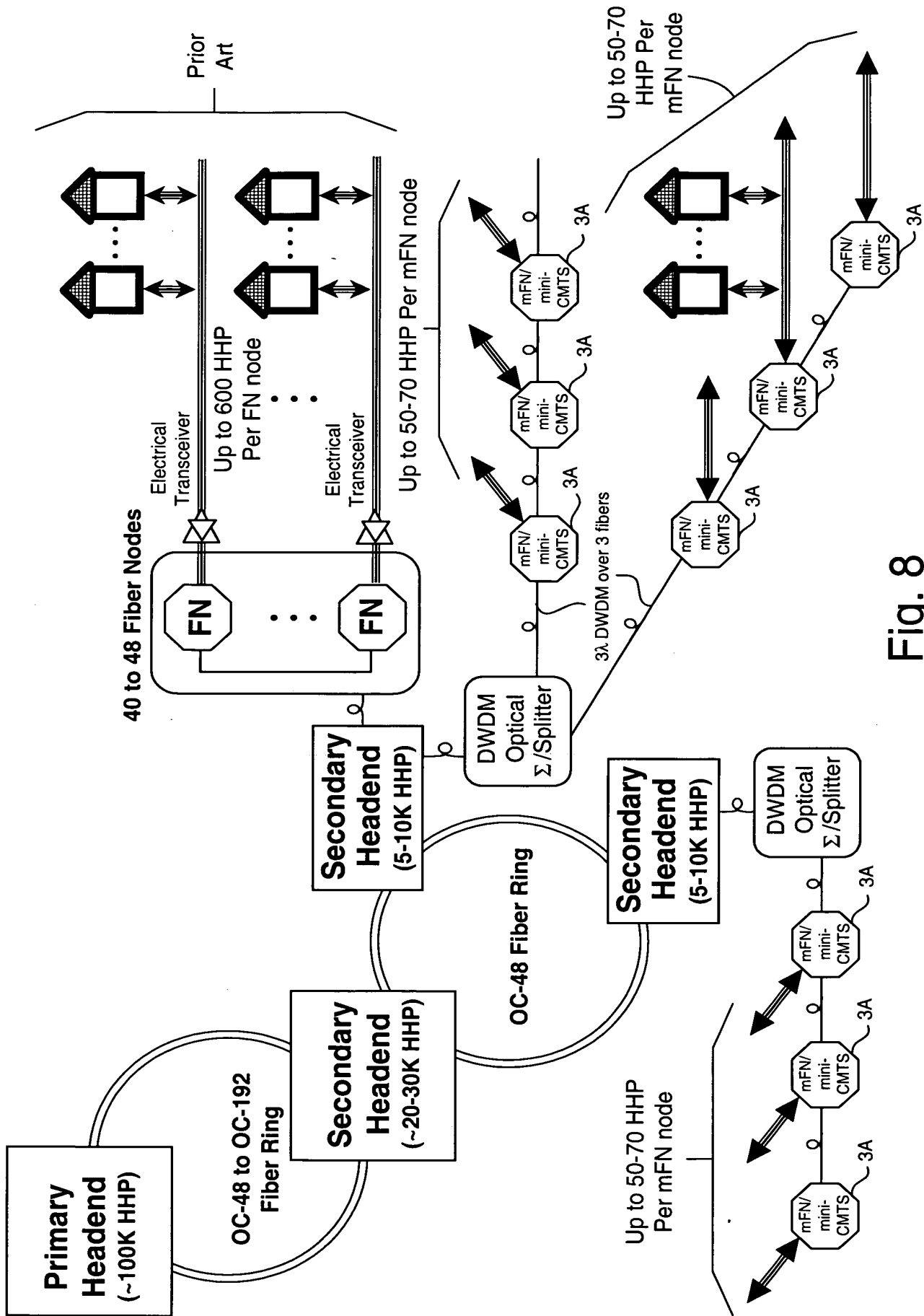


Fig. 8

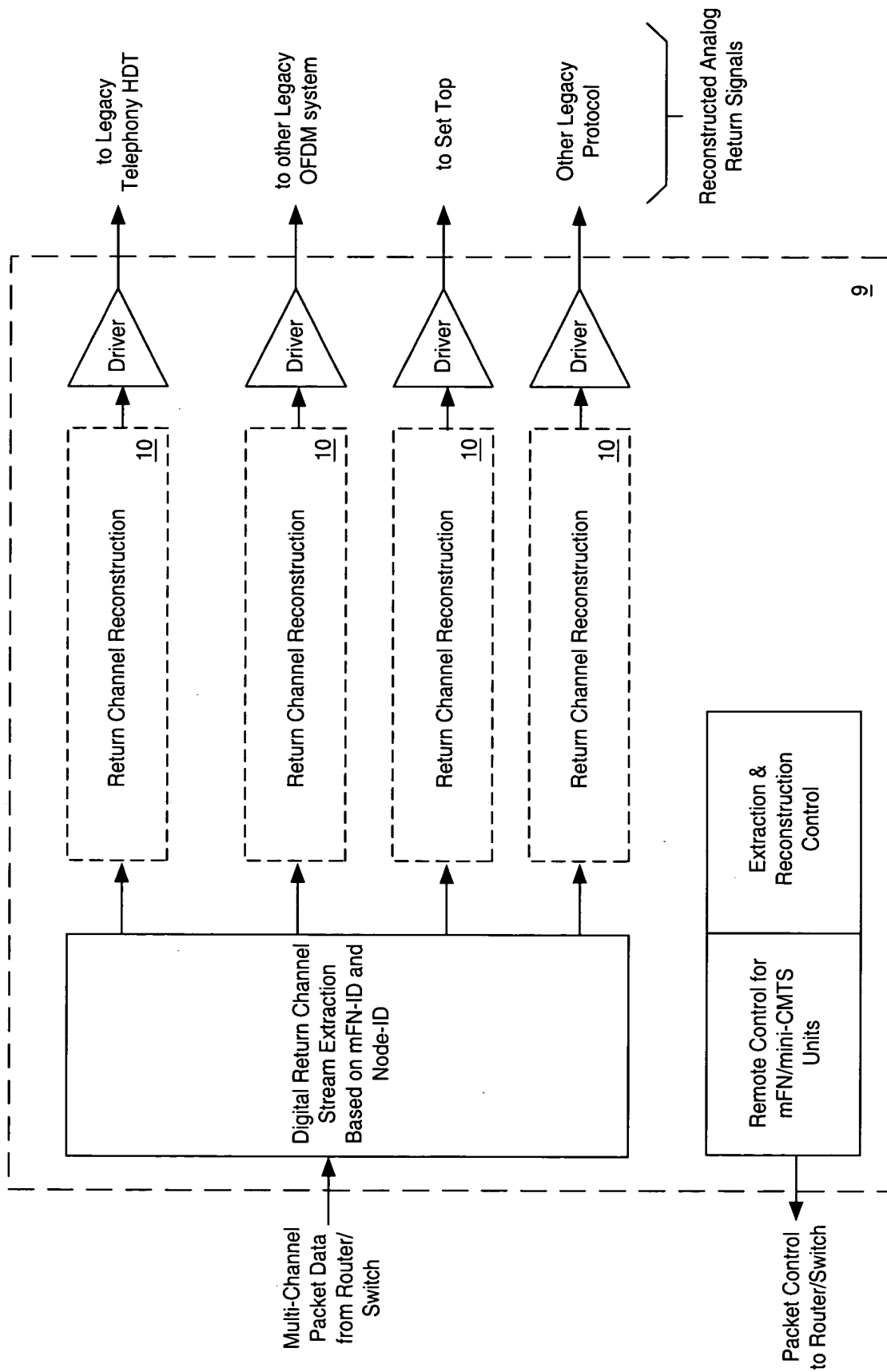


Fig. 9

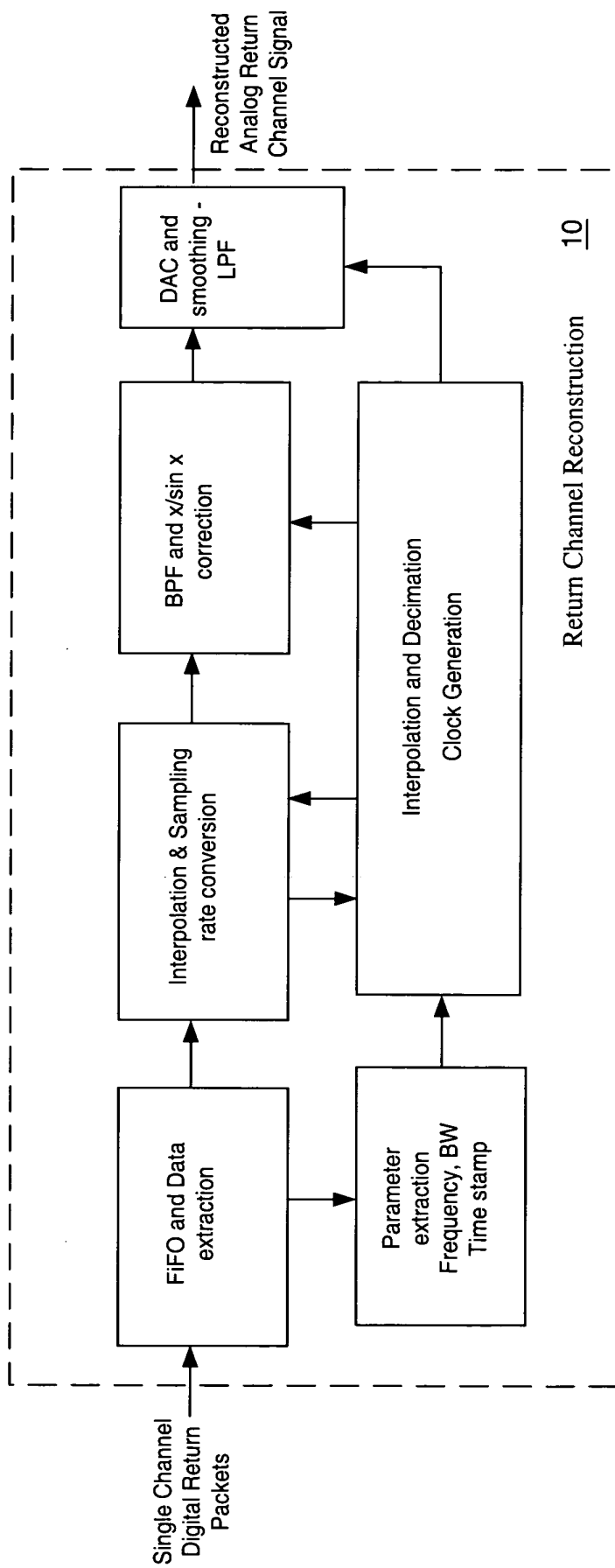
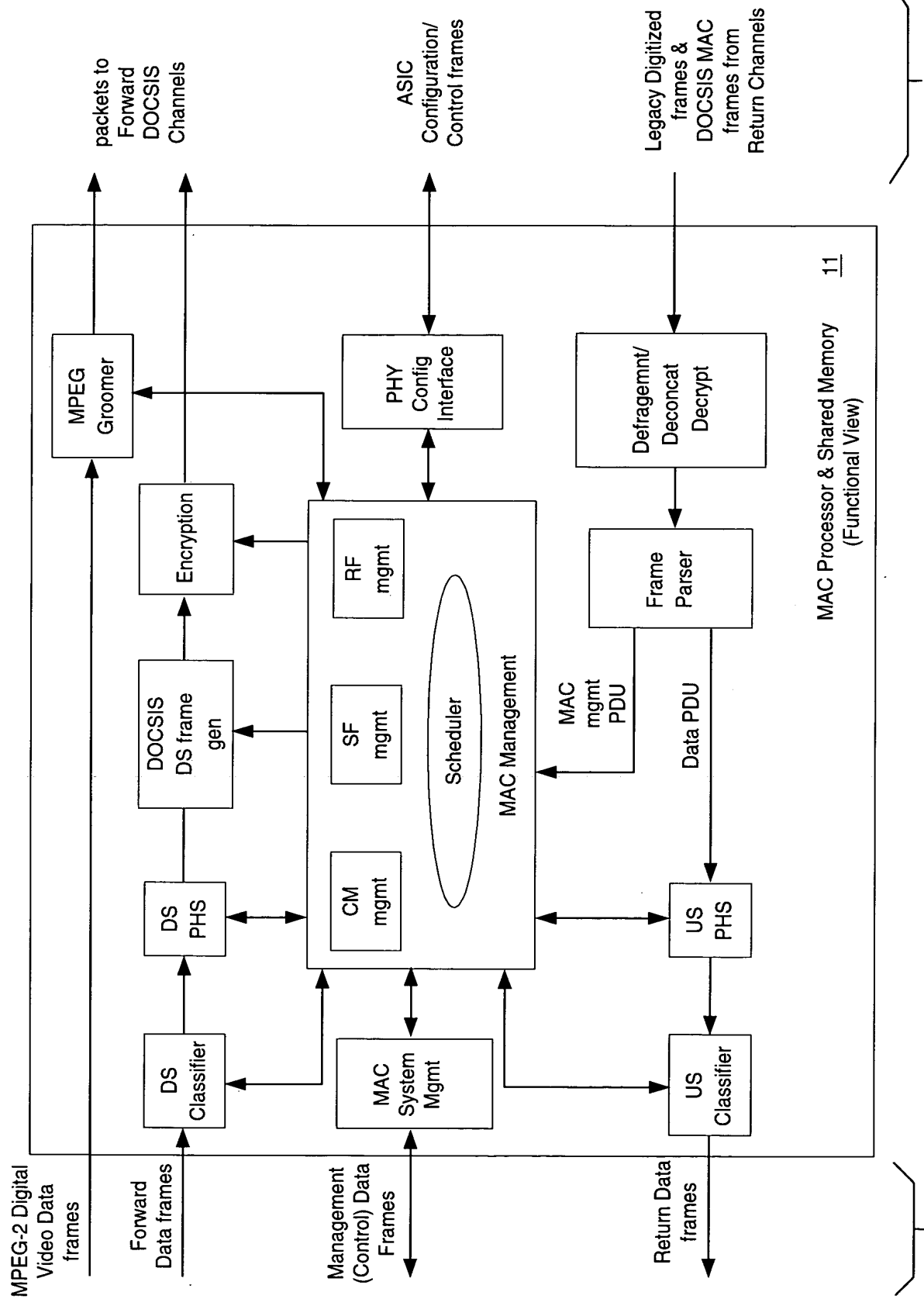


Fig. 10



From/To Primary Hub via Ethernet and O/E Interfaces

From/To ASIC via Multi-Master Bus

Fig. 11

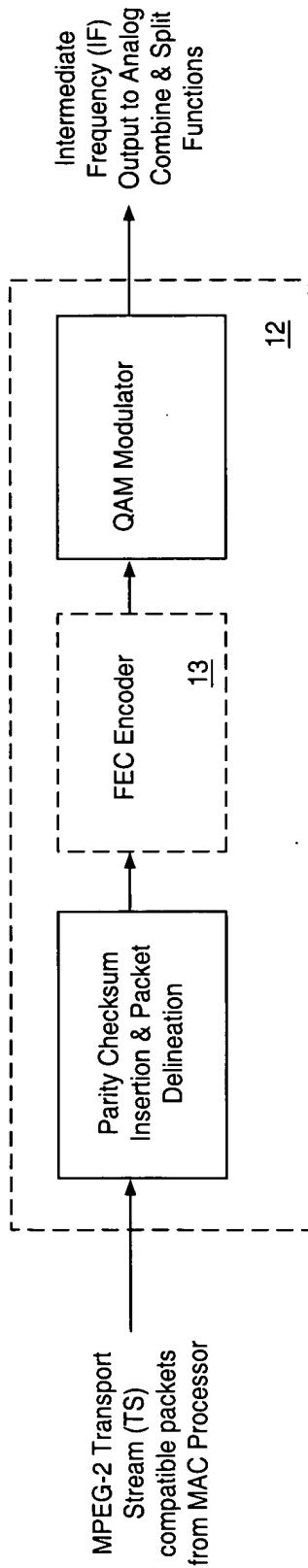


Fig. 12

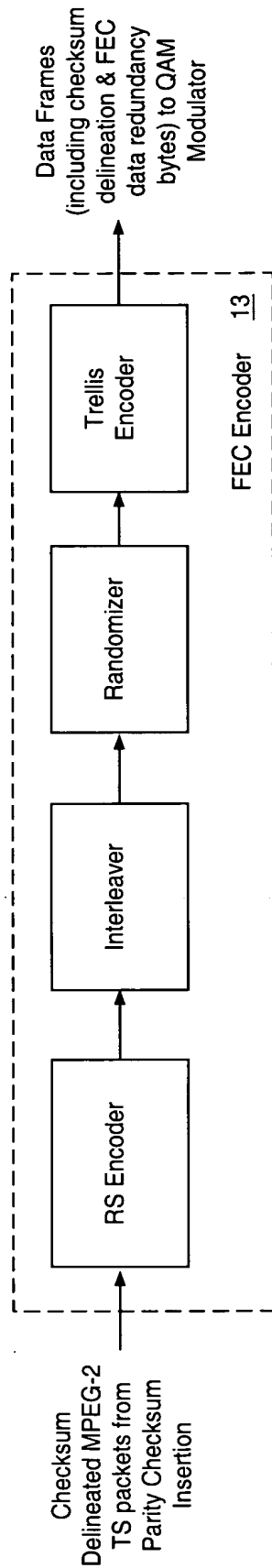


Fig. 13

U.S. Pat. No. 5,972,230

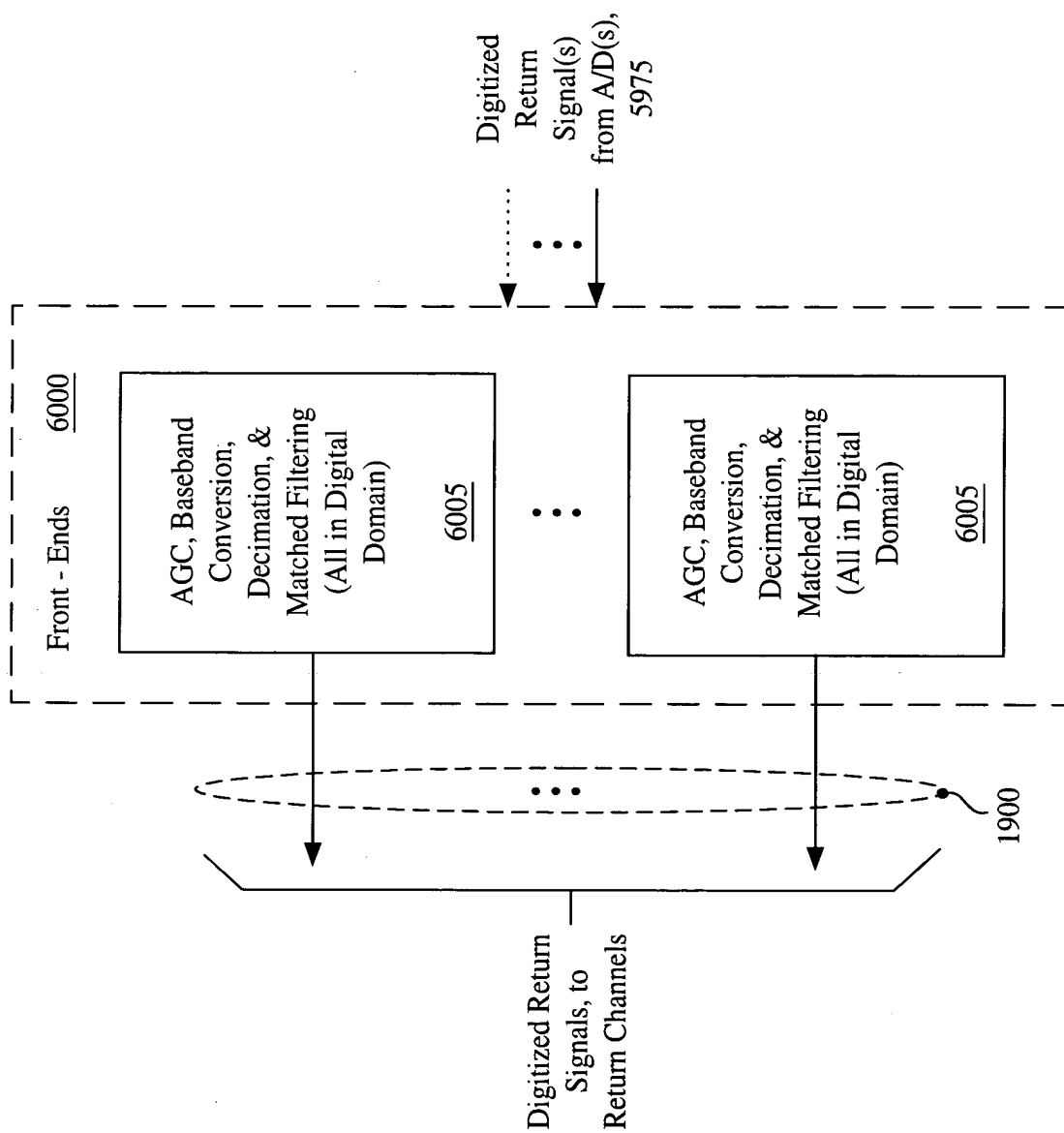


Fig. 14

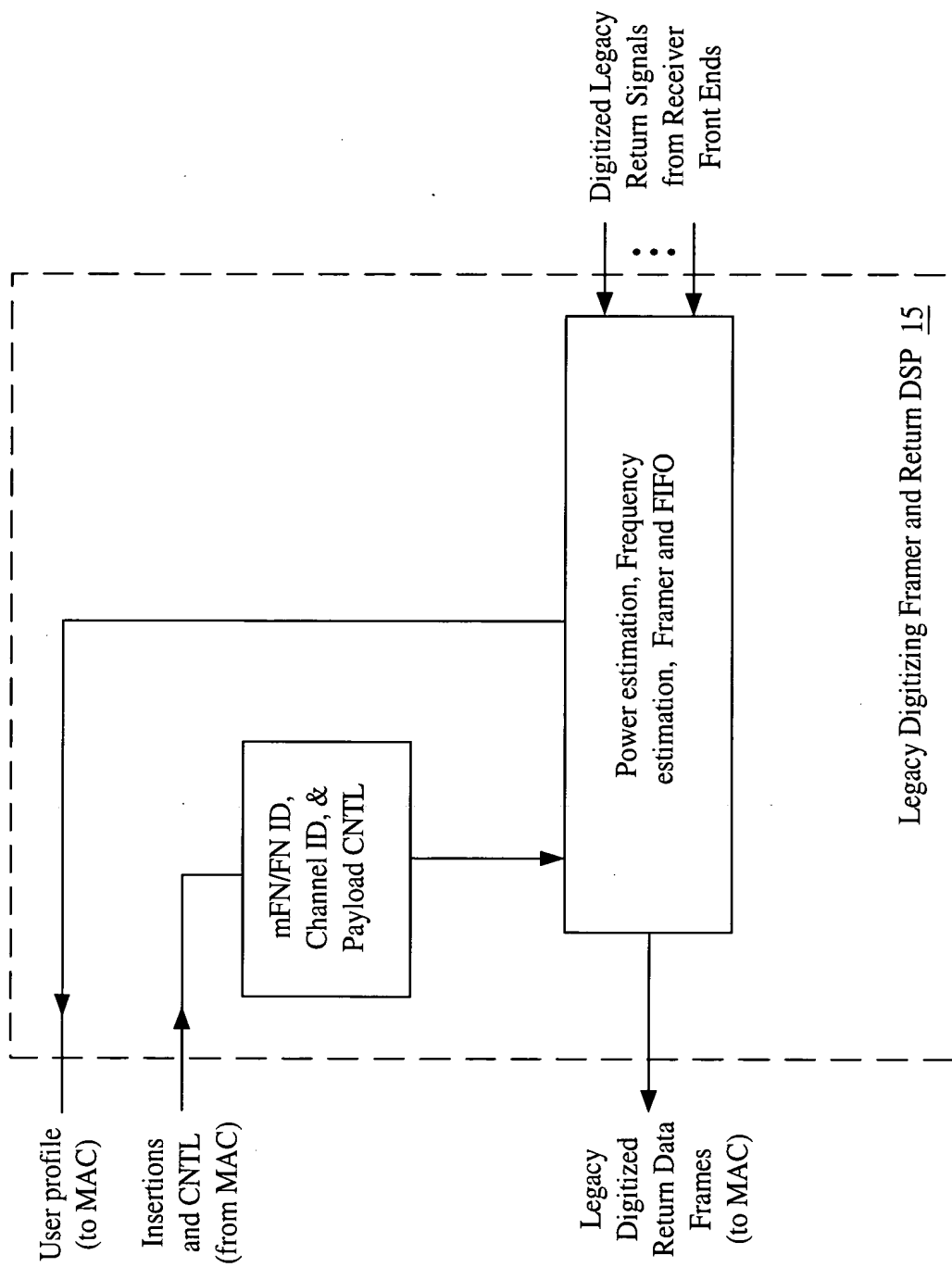


Fig. 15

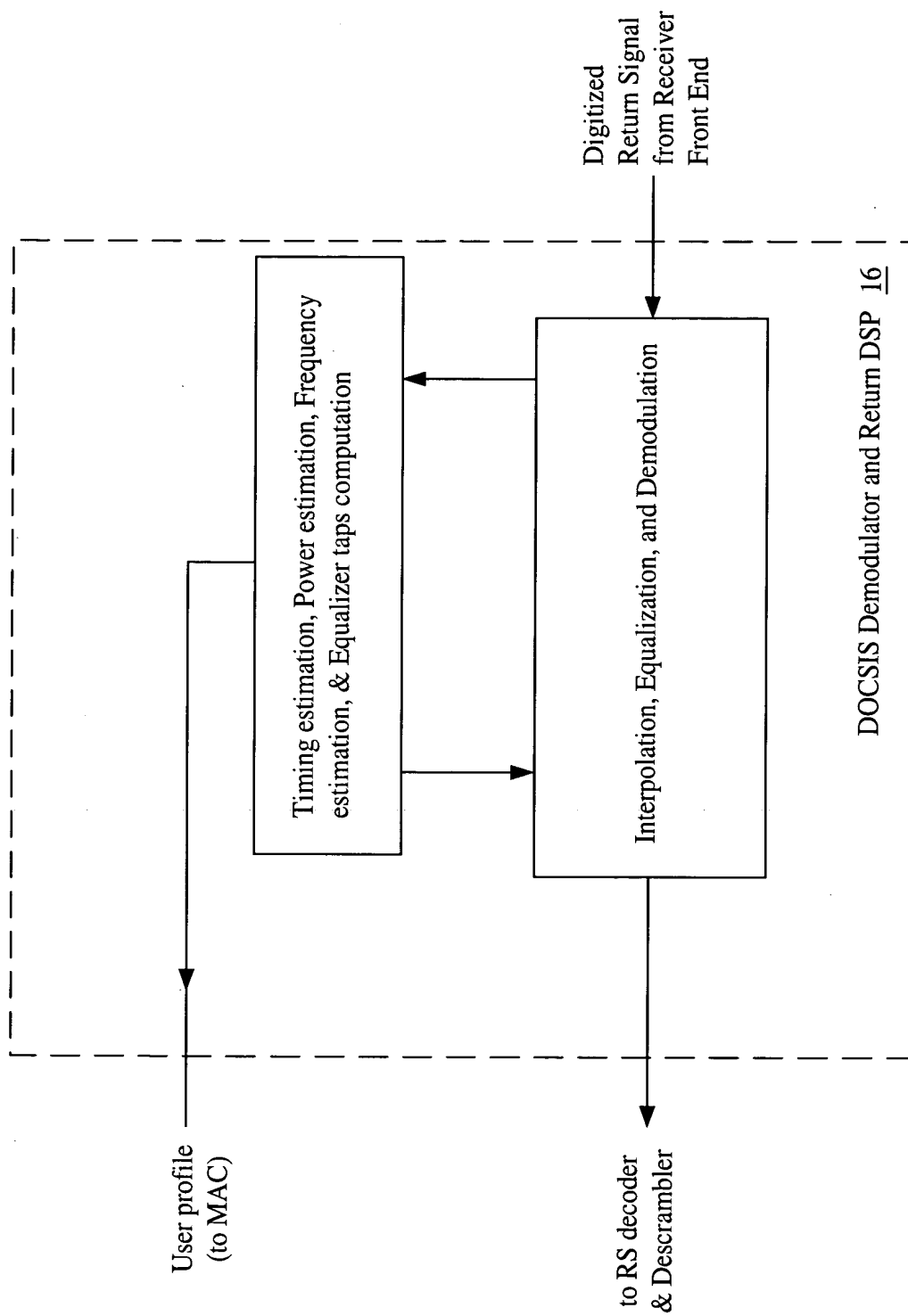


Fig. 16